AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. (Currently Amended) A method comprising:

~~frequency~~ dividing a high-frequency clock signal into a divided frequency signal in accordance with a data input; and

~~further~~ dividing said divided frequency signal into ~~another~~ a further divided frequency signal in accordance with ~~a~~ said data input ~~(DIN)~~.

2. (Currently Amended) The method according to claim 1, wherein ~~said further~~ dividing said divided frequency signal comprises dividing said divided frequency signal using ~~with~~ a multi-bit counter adapted to receive said data input ~~DIN~~ and to ~~further~~ divide said ~~clock~~ divided frequency signal in accordance with said ~~DIN~~ data input.

3. (Currently Amended) The method according to claim 1 ~~2 and further~~ comprising controlling at least one of dividing said high-frequency clock signal ~~said frequency dividing~~ and dividing said divided frequency signal ~~said further dividing~~.

4. (Currently Amended) The method according to claim ~~3~~ 1, wherein ~~said controlling~~ dividing said high-frequency clock signal comprises:

passing said high-frequency clock signal through a pass gate; and

sampling said high-frequency clock signal.

5. (Currently Amended) The method according to claim 4, wherein ~~said controlling~~ dividing said high-frequency clock signal further comprises, after said sampling, selectively closing said pass gate ~~at least once in a cycle associated with said high frequency clock signal~~ in accordance with a count value of said data input.

6. (Currently Amended) The method according to claim ~~4~~ 5, wherein said selectively closing comprises closing said pass gate if said count value is odd.

7. (Currently Amended) The method according to claim ~~3~~ 5, wherein said ~~controlling comprises controlling at least one of said high frequency clock signal and said data input with a~~ selectively closing comprises using at least one flip-flop ~~(FF)~~.

8. (Currently Amended) The method according to claim 1, wherein ~~said frequency~~ dividing said high-frequency clock signal comprises dividing said high-frequency clock signal ~~with a frequency divider that comprises~~ using a D-type flip-flop ~~(D-FF)~~ that feeds its Q-bar output into its data input.

9-16. Canceled.

17. (New) An apparatus comprising:

a frequency dividing arrangement adapted to divide a high-frequency clock signal into a divided frequency signal in accordance with a data input, and to divide said divided frequency signal into a further divided frequency signal in accordance with said data input.

18. (New) The apparatus of claim 17, wherein said frequency dividing arrangement comprises:

a frequency divider adapted to divide said high-frequency clock signal into said divided frequency signal;

a multi-bit counter adapted to divide said divided frequency signal in accordance with said data input; and

a control configuration to selectively pass said high-frequency clock signal to said frequency divider based on said data input.

19. (New) The apparatus of claim 18, wherein said frequency divider comprises a dual modulus frequency divider.

20. (New) The apparatus of claim 18, wherein said frequency divider comprises a D-type flip-flop that feeds its Q-bar output into its data input.

21. (New) The apparatus of claim 18, wherein said multi-bit counter comprises a 2n-bit counter adapted to receive data inputs DIN<1:(2^n-1)>.

22. (New) The apparatus of claim 18, wherein said control configuration is adapted to control a count precision of said multi-bit counter.

23. (New) The apparatus of claim 18, wherein said control configuration comprises a pass gate to be selectively closed based on a count value of said input data.

24. (New) The apparatus of claim 23, wherein said control configuration comprises at least one flip flop to selectively close said pass gate.

25. (New) The apparatus of claim 24, wherein said at least one flip flop is able to selectively close said pass gate based on an output of said multi-bit counter.

26. (New) An apparatus comprising:

a frequency dividing arrangement adapted to divide a high-frequency clock signal into a divided frequency signal in accordance with a data input, and to divide said divided frequency signal into a further divided frequency signal in accordance with said data input; and

an integrated circuit associated with said frequency dividing arrangement.

27. (New) The apparatus of claim 26, wherein said frequency dividing arrangement comprises:

a frequency divider adapted to divide said high-frequency clock signal into said divided frequency signal;

a multi-bit counter adapted to divide said divided frequency signal in accordance with said data input; and

a control configuration to selectively pass said high-frequency clock signal to said frequency divider based on said data input.